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Terms: **patno=5869353** ([Edit Search](#))

971499 (08) 5869353 February 9, 1999

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT
5869353

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February 9, 1999

Modular panel stacking process

REISSUE: Reissue Application filed Aug. 3, 2000 (O.G. Sep. 26, 2000) Ex. Gp.: 2812; Re. S.N. 09/633,297, (O.G. September 26, 2000)

INVENTOR: Levy, Aaron Uri, Stanton, CA; Sprint, John Patrick, Huntington Beach, CA; Forthun, John Arthur, Glendora, CA; Isaak, Harlan Ruben, Costa Mesa, CA; Mearig, Joel Andrew, Huntington Beach, CA; Calkins, Mark Chandler, Huntington Beach, CA

APPL-NO: 971499 (08)

FILED-DATE: November 17, 1997

GRANTED-DATE: February 9, 1999

ASSIGNEE-AT-ISSUE: Dense-Pac Microsystems, Inc., Garden Grove, CA

ASSIGNEE-AFTER-ISSUE: November 17, 1997 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., DENSE-PAC MICROSYSTEMS, INC. 7321 LINCOLN WAY GARDEN GROVE CALIFORNIA 92641, Reel and Frame Number: 008832/0596

LEGAL-REP: Loeb & Loeb LLP; Scherlacher, John P.

PUB-TYPE: February 9, 1999 - Utility Patent having no previously published pre-grant publication (A)

PUB-COUNTRY: United States (US)

US-MAIN-CL: 438#109

US-ADDL-CL: 438#110, 438#111, 438#113


CL: 438

SEARCH-FLD: 438#113, 438#111, 438#110, 438#109, 438#366, 438#368

IPC-MAIN-CL: H 01L021#44

IPC ADDL CL: H 01L021#48, H 01L021#50

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patno=5869353

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US 5,869,353

09/633297

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Search statement 1

?us5869353/pn

** SS 1: Results 1

Search statement 2

?prt fu legalall max

1/1 PLUSPAT - (C) QUESTEL-ORBIT- image
CPIM (C) Questel-Orbit
PN - US5869353 A 19990209 [US5869353]
TI - (A) Modular panel stacking process
PA - (A) DENSE PAC MICROSYSTEMS INC (US)
PA0 - Dense-Pac Microsystems, Inc., Garden Grove CA [US]
IN - (A) LEVY AARON URI (US); SPRINT JOHN PATRICK (US); FORTHUN JOHN
ARTHUR (US); ISAAK HARLAN RUBEN (US); MEARIG JOEL ANDREW (US);
CALKINS MARK CHANDLER (US)
AP - US97149997 19971117 [1997US-0971499]
PR - US97149997 19971117 [1997US-0971499]
IC - (A) H01L-021/44 H01L-021/48 H01L-021/50
EC - H01L-021/98
- H01L-025/10J
- H05K-001/14D
- H05K-001/18C
PCL - ORIGINAL (O) : 438109000; CROSS-REFERENCE (X) : 438110000 438111000
438113000
DT - Basic
CT - US4956694; US5313096; US5466634; US5612570; JP56-88324
- Ghandhi, Sorab K., VLSI Fabrication, John Wiley & Sons, Inc. p. 641,
1994.
STG - (A) United States patent
AB - A method of making chip stacks begins with the formation of a
plurality of panels having apertures therein and conductive pads on
opposite sides thereof. Solder paste is deposited on the conductive
pads prior to mounting plastic packaged IC chips within each of the
apertures in each of the panels so that opposite leads thereof reside
on the conductive pads at opposite sides of the apertures. The plural
panels are then assembled into a stack, such as by use of a tooling
jig which aligns the various panels and holds them together in
compressed fashion. The assembled panel stack is heated so that the
solder paste solders the leads of the packaged chips to the conductive
pads and interfacing conductive pads of adjacent panels together, to
form a panel stack comprised of a plurality of chip package stacks.
Following cleaning of the panel stack to remove solder flux residue,
the individual chip package stacks are separated from the panel stack
by cutting and breaking the stack. Score lines across a topmost panel
and transverse slots within remaining panels therebelow result in the
formation of strips of chip package stacks when longitudinal cuts are

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made through the panel stack. The remaining portions of the uppermost panel within such strips are then snapped along the score lines thereof to separate the individual chip package stacks from the strips.

1/1 LGST - (C) LEGSTAT
PN - US 5869353 [US5869353]
AP - US 971499/97 19971117 [1997US-0971499]
DT - US-P
ACT - 19971117 US/AE-A
APPLICATION DATA (PATENT)
{US 971499/97 19971117 [1997US-0971499]}
- 19971117 US/AS02
ASSIGNMENT OF ASSIGNOR'S INTEREST
DENSE-PAC MICROSYSTEMS, INC. 7321 LINCOLN WAY GARDEN GROVE, CALIFORNIA
92641-142 * LEVY, URI AARON : 19971107; SPRINT, JOHN PATRICK :
19971107; FORTHUN, JOHN ARTHUR : 19971107; ISAAK, HARLAN RU : 19971107;
- 19990209 US/A
PATENT
- 20000926 US/RF
REISSUE APPLICATION FILED
20000803
UP - 2000-40

1/1 CRXX - (C) CLAIMS/RRX
AN - 3108897
PN - 5,869,353 A 19990209 [US5869353]
PA - Dense-Pac Microsystems Inc
PT - C (Chemical)
ACT - 20000803 REISSUE REQUESTED
Issue Date of O.G.: 20000926
Reissue Request Number: 09/633297
Examination Group responsible for Reissue process: 2812

UP - 2000-39
UACT- 2000-09-26

1/1 PAST - (C) Thomson Derwent
AN - 200039-002241
PN - 5869353 A [US5869353]
DT - A (UTILITY)
OG - 2000-09-26
CO - REA
ACT - REISSUE APPLICATION FILED
SH - REISSUE APPLICATION FILED

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Search statement 1

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1 Patent Groups
** SS 1: Results 1

Search statement 2

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1/1 INPADOC - (C) INPADOC
PN - US 5869353 A 19990209 [US5869353]
TI - MODULAR PANEL STACKING PROCESS
IN - LEVY AARON URI [US]; SPRINT JOHN PATRICK [US]; FORTHUN JOHN ARTHUR
[US]; ISAAK HARLAN RUBEN [US]; MEARIG JOEL ANDREW [US]; CALKINS MARK
CHANDLER [US]
PA - DENSE PAC MICROSYSTEMS INC [US]
AP - US 971499/97-A 19971117 [1997US-0971499]
PR - US 971499/97-A 19971117 [1997US-0971499]
IC - H01L-021/44; H01L-021/48; H01L-021/50

1/1 LEGALI - (C) LEGSTAT
PN - US 5869353 [US5869353]
AP - US 971499/97 19971117 [1997US-0971499]
DT - US-P
ACTE- 19971117 US/AE-A
APPLICATION DATA (PATENT)
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